IN THE CLAIMS:

Please cancel claims 1, 2, 4, 8-10, and 12. **Please also amend** claims 3, 5, 11 and 13 as shown in the complete list of claims that is presented below.

Claims 1 and 2 (cancelled).

3. (currently amended): A dry etching method for a semiconductor device, comprising the following steps of:

simultaneously gate-etching an N type polysilicon gate [[and]] electrode, a P type polysilicon gate electrode, and a non-doped polysilicon body during a two-stage etching process; and

setting an etching area occupied by [[a]] the non-doped polysilicon body, which is adjacent to at least one of the N type polysilicon gate electrode and the P type polysilicon gate electrode, larger than a total area of the N type polysilicon gate electrode and the P type polysilicon [[gate.]] gate electrode,

wherein an end point detection of one of the stages of the etching process is based on the etching of the non-doped silicon body.

Claim 4 (cancelled).

5. (currently amended): The dry etching method according to claim [[4]] 3, wherein the two-stage etching includes a first stage using a mixed gas of HBr and O_2 and a second stage using a mixed gas of HBr, O_2 and He.

Claims 6-10 (cancelled).

11. (currently amended): The dry etching method according to claim 3, wherein the N type polysilicon gate electrode and the P type polysilicon gate electrode are disposed adjacent one another.

Claim 12 (cancelled).

13. (currently amended): The dry etching method of claim 3, wherein the N type polysilicon gate electrode, the P type polysilicon gate electrode, and the non-doped polysilicon body are all etched ~~simultaneously~~ from a single polysilicon layer.